IN THE CLAIMS

Please Amend Claim 1 As Follows.

1. (**Currently Amended**) In a timing trace stream having a logic signal associated with each clock cycle, the timing trace stream being transmitted in ~~packets~~ packet groups having a plurality of packets, a method of compressing the timing trace stream, the method comprising:

when each of a preselected number of clock cycles have at least one logic "1" signal and at least one logic "0" signal associated with each clock cycle, transmitting a standard group of packets having a logic signal associated with each of the preselected number of clock cycles; ~~and~~

when the preselected number of clock cycles has only one of the logic "1" and the logic "0" signals associated with each clock cycle, transmitting a compressed group of packets, the packets including an indicia of the one logic signal, the packets including a signal group representing the preselected number;

wherein each group of packets has at least one header packet and at least one information packet; and

wherein the standard group of packets includes a plurality of information packets and the compressed group of packets includes one information packet.

Please Cancel Claim 2.

2. (**Currently Cancelled**) ~~The method as recited in claim 1 wherein each group of packets has at least one header packet and at least one information packet.~~

Please Cancel Claim 3.

3. (**Currently Cancelled**) ~~The method as recited in claim 2 wherein the standard group of packets includes a plurality of information packets and the compressed group of packets includes one information packet.~~

Please Amend Claim 4 As Follows.

4. (**Currently Amended**) The method as recited in claim 1 further comprising:

representing an activity of ~~the~~ a program counter with a first logic signal during a clock cycle; and

representing a non-activity of the program counter with a second logic signal during ~~an associated~~ a clock cycle.

Please Amend Claim 5 As Follows.

5. (**Currently Amended**) An apparatus for generating a timing trace stream in a target processor, a logic signal being associated with each target processor clock cycle, the apparatus comprising;

a logic unit responsive to a preselected number of logic signals, the logic unit providing a first control signal when all the preselected logic signals are different, the logic signal providing a second control signal when all the preselected logic signals are the same;

a first storage unit responsive to the preselected logic signals for storing the each logic signal in a predetermined storage location, the first storage unit responsive to the first control signal for transferring the contents of then first storage unit; ~~and~~

A second storage unit responsive to the preselected logic signals for storing the current logic signal in a pre-established storage unit location, the second storage unit storing a signal group representing a multiple of the preselected number, the second storage unit responsive to the second logic signal for transferring the contents of the second storage unit; and

wherein the storage location in the first and the second storage units are arranged in groups of packets, each group of packets including control signals with the packet payload.

Please Cancel Claim 6.

6. (**Currently Cancelled**) ~~The apparatus as recited in claim 5 wherein the storage location in the first and the second storage units are arranged in groups of packets, each group of packets including control signals with the packet payload.~~

Please Amend Claim 7 As Follows.

7. (**Currently Amended**) The apparatus as recited in claim 5 wherein each of the preselected number of logic signals represents an activity of ~~the~~ a program counter during an associated clock cycle.

8. (**As Filed**) The apparatus as recited in claim 5 further comprising a first in/first out storage unit, the contents of the first and the second storage unit being transferred to the first in/first out storage unit.

Please Amend Claim 9 As Follows.

9. (**Currently Amended**) A system for transferring data concerning the operation of target processor to a host processing unit, the system comprising:

a program counter trace stream generation unit, the program counter trace stream generation unit generating a trace stream identifying each activity of the program counter; and

a timing trace stream generation unit, the timing trace stream generation unit having a first mode of operation generating a timing trace header packet and a first information packet stream with a logical signal associated each clock cycle, ~~the~~ a first logical signal identifying when the program counter performed an activity during the associated clock cycle and a second logic signal identifying when the program counter was non-active during an associated clock cycle, the timing trace stream

generation unit having a second mode of operation generating a header packet and a second timing trace information packet, the second timing trace information packet replacing at least one first information packet when all of the logic signals in the at least one first information packet ~~including one type of signal group relating a~~ are the same logic signal ~~with each of a predetermined number of clock cycles~~, ~~the timing trace stream including a second type of signal groups identifying the predetermined number of clock cycles having the same logic signal~~ the timing trace generation unit including a logic unit, the logic unit generating control signals determining whether the first information packet stream or the second information packet is transferred to the host processing unit.

Please cancel Claim 10.

10. (**Currently Cancelled**) ~~The system as recited in claim 9 wherein the trace streams include header packets and information packets.~~